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EXAMINER
~~TEAM EXAM 61X~~

E6M1/1122

ART UNIT	PAPER NUMBER
2613	5

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DATE MAILED: 11/22/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 9/18/95 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 21-97 are pending in the application.

Of the above, claims _____ are withdrawn from consideration.

2. ☒ Claims 1-20 have been cancelled.

3. ☐ Claims _____ are allowed.

4. ☒ Claims 21-97 are rejected.

5. ☐ Claims _____ are objected to.

6. ☐ Claims _____ are subject to restriction or election requirement.

7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. ☐ Formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).

10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).

12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.

13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

Part III DETAILED ACTION

This application has been examined by a team of three Examiners as part of a pilot team-examining program within the U.S. Patent Office.

1. As the previous Office Action crossed in the mail with applicant's preliminary amendment, this Action supplements and effectively replaces said previous Action and restarts the period for response. Applicant, however, is requested to make note of said previous Action and to be made aware that the statements advanced in the previous Action with regard to the references applied in this Action are equally applicable.

2. Copies of references relied upon herein and not supplied herewith can be found in one or more of applicant's priority of co-pending applications. Therefore, in the interest of expediency and conservation, copies of these references are not being again supplied since applicant already has one or more such copies.

3. Claims 21-97 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 24, 25, 57 and 63 are vague and indefinite because they depend from cancelled parent claims.

The dependent claims are replete with instances of terms for which there is no clear antecedent. Many of the dependent claims appear to depend from the wrong parent claim. It is suggested that all of the claims be carefully and thoroughly reviewed for the proper dependencies.

Claim 21 is incomplete. The claim recites two independent and distinct systems not joined in any way. The claim specifies an "image memory" coupled to a "processor," then a "plurality of memories" coupled to one "input circuit" and two "output circuits." There is no connection recited between the "image memory" and the subsequent "plurality of memories."

In claim 26, "an input circuit generating a sequence of input words in response..." is vague and indefinite: What information is contained in the "input words"? It is impossible to determine whether these words are sub-units of previous image information, or if they represent information extracted from previous image information, or if they represent something else entirely. Also, absent clarification of the nature of this "input word" information, there does not appear to be any clear connection between the "image memory/processor" and the rest of the claimed apparatus.

In claim 31, "forth memory" is vague and indefinite: The meaning of the term "forth" cannot be ascertained. Also claim 31 is incomplete. The claim recites independent and distinct systems not joined in any way. The claim specifies an "image memory" coupled to a "processor," then a "plurality of memories" coupled to one "input circuit" and one "output circuit." There is no connection recited between the "image memory" and the subsequent "plurality of memories." Also there is no connection between the "input circuit/first memory" and the remaining three "memories/output circuit".

In claim 33, "spatially filtered" is vague and indefinite. This is an implied limitation since no "spatial filter" is recited.

Claim 36 is essentially identical to claim 31 and is rejected for the same reasons. This claim also adds a "kernel processor" which is connected to the remaining three "memories/output circuit" which is not connected in any way to the "image memory/processor" or the "input circuit/first memory."

In claim 37, "an input circuit... storing a sequence of input words into the input memory..." is vague and indefinite: What information is contained in the "input words"? It is impossible to determine whether these words are sub-units of previous image information, or if they represent information extracted from previous image information, or if they represent something else

entirely. Also, absent clarification of the nature of this "input word" information, there does not appear to be any clear connection between the "image memory/processor" and the rest of the claimed apparatus.

In claim 46, a "triple line buffer... storing three lines of display information in response to the input line of display information..." is vague and indefinite: This makes no sense. It is not possible to store three lines of information in a device when only a single line of information is input to the device. Even if the single line is stored in three places, it remains the same single line of information, ie, no new lines of information are created. "The double buffered triple line buffer" lacks antecedent.

Claims 51 and 52 are essentially identical to claim 46 and are rejected for the same reasons, except that "double buffered triple line buffer" has an antecedent.

In claim 58, "an input circuit generating an input line of display information" is vague and indefinite: It is not clear whether the term "line" refers to a data line, ie, a wire, or to a sequence of data. "A first line" and " a second line" are also vague for the same reason. Also this claim is incomplete. The claim recites a linear progression of elements that does not have any determinable function or end. An image is input to a first

buffer, accessed, input to a second buffer, and accessed. Processing takes place before these "accessings" therefore their functions cannot be determined.

Claim 60 is essentially identical to claim 58, but adds a "third line buffer/accessing circuit." This claim is rejected for the same reasons as claim 58.

In claim 65, "an input circuit generating a sequence of input words in response..." is vague and indefinite: What information is contained in the "input words"? It is impossible to determine whether these words are sub-units of previous image information, or if they represent information extracted from previous image information, or if they represent something else entirely. Also, absent clarification of the nature of this "input word" information, there does not appear to be any clear connection between the "image memory/processor" and the rest of the claimed apparatus. Further, in line 11, the term "simultaneous" is unclear as to what is "simultaneous" with what.

Also there is no meaningful interconnection between the input, output and plurality of memories. "Precessing the plurality of memories between an input memory ... and a plurality of output memories" is incomprehensible. In addition it is not clear how if at all "precessing memories" involves "input" and "output."

In claim 70, "an input circuit generating input words in response..." is vague and indefinite: What information is contained in the "input words"? It is impossible to determine whether these words are sub-units of previous image information, or if they represent information extracted from previous image information, or if they represent something else entirely. Also, absent clarification of the nature of this "input word" information, there does not appear to be any clear connection between the "image memory/processor" and the rest of the claimed apparatus. Also, "address control signal," "input control signal" and "output control signal" lack antecedent. Are these signals supplied by the operator or by the apparatus?

Claim 75 is essentially identical to claim 70 except that "precessional" control signals are recited. This claim is rejected for the same reasons as claim 70. In addition, the term "precessing" is incomprehensible as used in various forms in the claim.

Claim 80 is incomplete. The "image memory/processor" and "frame buffer/accessing circuit" are in no way connected to the apparatus that follows. "The output circuit" of the second clock circuit has no clear antecedent--three output circuits have been recited.

In claim 81, "input words" and "output words" are vague and indefinite: These terms lack a clear antecedent or definition in the claims. "Words" can refer to either information stored in the image memory or to other information. Also, there is no connection between the steps of "writing" and "outputting."

In claim 82, "input words" and "output words" are vague as in claim 81. "Words of information," "a plurality of sequences" and "the first buffer" have no antecedent in the claim.

In claims 83 and 84, "input words" and "output words" are vague as in claim 81. "Forth memory" is undefined. "The input circuit" has no antecedent.

In claim 85, "input words" and "output words" are vague as in claim 81. "An input memory" and "an output memory" have no antecedent or definition.

In claim 86, "line of information" is vague. This can mean communication line, or a line of text, or something else.

In claims 87 and 88, "line of information" is vague as in claim 86. "Double buffered display information" has no antecedent.

In claims 89 and 90, "line of information" is vague as in claim 86.

Claim 91 is unintelligible. "Words" is undefined as in claim 81. It is not possible to determine whether "words" are generated as input or output.

In claim 92, "input words" and "output words" are vague as in claim 81. "Informational image information" is meaningless. "Storing words" is vague: Input or output words? "Input control signal," "output control signal" and "address control signal" have no antecedent or definition in the claim.

In claim 93, "input sequence of words" and "output sequence of words" are vague as in claim 81. "Storing a sequence words" is vague: Input or output words? "Input-" and "output precessional control signal" have no antecedent in the claim.

Claim 94 is unintelligible. "Making a product" is meaningless in the context of an image processing system as described. Also, it is not clear that the specification contains support for producing a product.

In claim 96, "database memory" and "image memory" are vague. Since the "database memory" stores an "image" it is also an "image memory," thus two different terms are used to describe the same thing.

In claim 97, "scanning out" is vague and indefinite. It is not clear whether this means "reading from memory" or something else.

4. In view of the numerous ambiguities in the claims and specification, as indicated in paragraph 3, above, the claims are

interpreted as best that they are understood, and the prior art is applied (in paragraphs 5-18, below) in accordance with this understanding.

5. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 21-24, 26-29, 31-34, 36-41, 43-49, 51-56, 58-63, 65-68, 70-73, 75-78, 80-97, as best that they are understood, are rejected under 35 U.S.C. § 103 as being unpatentable over Marsh (4,179,824).

6. It is noted that the claims broadly recite various types of processing, where the processing is simply inserted as a one (or two) word adjective to describe the processing (such as the processor generating "clipped" image information or "composite" image information). There is no further recitation directed to the specifics of the processing being performed in any of the numerous

claims. Therefore, the claims will firstly be addressed with respect to the system (or method) without specific reference to the recited type of processing, and later addressed as to the recited processing, as it appears that the type of processing is, at best, a secondary, if not immaterial, part of applicant's actual invention. This is further supported by the fact that applicant has filed approximately 40-50 applications with nearly identical claims, with the only claimed differences therebetween being the broad recitation of different processes being performed by the processor (as well as the use of a database memory, an image memory, or no memory prior to the processor, which will be addressed below).

7. With general regard to the independent claims, Marsh discloses a system for processing images, comprising: storing image data in a database memory (48); extracting image data from the database and storing it in an image memory; using a processor to process the image data, where the processing includes translation, rotation, scaling, compression (reduction), expansion, texture, topography, map, roll, pitch, occulting, perspective, and 3D image production; means for transmitting the processed data from the processor to at least one of a plurality of further memories (Where the means, while not explicitly shown, is inherent, as the processed data is clearly sent to the memory and there must be a means to perform

this function. Further, this would be readable on the various claim recitations directed to an input circuit and accessing means for addressing the memory, as for data to be stored and read from a memory, there must be these types of means. These means for storing to and reading from a memory are inherent in any system that perform these functions.); and means for reading out the memory that has data stored therein (Which, like the means for inputting data into the memory, is also inherent, as there must be such means to allow the data in the memory to be read out. These inherent means would correspond to applicant's variously recited output circuits and output accessing circuits.). Further, since Marsh discloses a system using a database memory and an image memory to provide image data to the processor, this would satisfy claims that recite a system "comprising" all three of these elements, as well as systems that recite only one or neither of the memories.

8. Further, and with more specificity towards the various independent claims, the system Marsh discloses comprises: a data base memory (48) in Fig. 1; an image memory (304, 306, in Fig. 3, makes up part of element 46 in Figs. 1 and 3) for storing an image (where the image is accessed from part of the data base 48); a processor (comprising elements 60, 60C, 62, 63, 64, 65 and 72 in Fig. 1, and referred to more specifically in subsequent Figs.) for

processing the image stored in the memory, where the processor performs the following processes: translation, rotation, scaling, compression (reduction), expansion, texture, topography, map, roll, pitch, occulting, perspective, and 3D image production; an input circuit for accessing the image from the processor (This is an inherent operation and means as the data must have some way to be taken from the processor to the memory, which is clearly happening in the reference. Further, the processor control logic 70 in Fig. 1 would also apparently satisfy the limitations in the claims. Also, see column 3, lines 10-12.) and storing the data in a memory; a plurality of memories (Each separate processing section 60-65 contains its own memory and means to address the respective memory. For example, Fig. 3 shows RAM 304 and buffer 306, as well as RAM 350 which is accessed by the addressing circuit 320. The other Figs. show similar means.); and a display processor to process and display the processed image (72, 74, 76, 82 in Fig. 1). Further, see: Abstract; Figs. 1-11; column 1, lines 6-14, 31-51; column 2, line 21 to column 3, line 41, particularly column 2, lines 29-34, 35-43, 54-66, and column 3, lines 1-19, 26-31; column 4, line 21 to column 5, line 52 (which discusses producing processed images at varying resolutions); column 6, lines 28-68; column 7, lines 55-68; column 8, lines 14-27, 44-49; column 9, lines 29-62; column 10, lines 23-50; column 11, line 13-52; column 12, line 49 to column

13, line 57, particularly column 12, lines 65-68 and column 13, lines 54-57; column 16, lines 53-68; column 28, lines 23-43; column 29, lines 36-60; column 31, line 60 to column 33, line 8; and column 36, line 55 to column 37, line 17.

9. With respect to the variously recited processes recited in the various independent claims, it is firstly noted that Marsh shows many of these transformations (including translation, rotation, scaling, compression (reduction), expansion, texture, topography, map, roll, pitch, occulting, perspective, and 3D image production, as indicated above). The use of these transformations, or any of the other extremely well-known and conventional processes that are broadly and generically recited in the claims, would have been obvious to one of ordinary skill in the art because of the conventionality of these processes and because Marsh already shows performing many of the recited transformations (Official Notice). Further, since there are no recited specifics in the claims of the transformations, these are simply a generic statement of a well-known process and the use of any one in place of any of Marsh is simply the matter of substituting one well-known process with another, and, in some instances, simply the matter of reciting a broader version of what Marsh discloses (such as "geometric" rather than "rotation", "translation" or "scaling").

10. With respect to the claim recitation in a number of the claims of storing data in a first memory while data is being read out of a second memory, it is firstly noted that Marsh discloses (Fig. 1) an image processor (42) that is comprised of a plurality of processes (60-65), which are apparently performed in succession, which suggests a pipelined processing, as this is apparently what is being performed (i.e., the rotation processor (62) is operating on data already processed by the translation processor (60), while the rotation processor is operating on subsequent data. Therefore, the operations are pipelined and simultaneous.). Further, the process of performing write operation to a first memory simultaneously with the reading out of a second memory is a very well-known process to enhance the processing speed of the system. Further, since Marsh apparently suggests a pipelined process, the use of such procedures to increase the operating speed of the system is clearly desirable in Marsh. Therefore, to one of ordinary skill in the art, it would have been obvious, at the time of the invention, to perform the write and read operations simultaneously so as to increase the operational speed of the system.

11. With respect to the claims (such as 26, 46 and others) that recite the use of various buffers, double buffers and triple line buffers, these are all well known memory devices for the storage of

data, particularly the storage of kernels or windows of image data to allow the processing of small amounts of data (Official Notice). The use of these types of devices in the system of Marsh would have been obvious to one of ordinary skill in the art because of the conventionality of the use of these devices and because Marsh shows the use of various buffers, registers and memories throughout his system (such as elements 306, 304 and 310, for example). With respect to the claims (such as 37 and 70) that recite the use of a selector or multiplexer for selecting the memory device that is to be read into or read out of by the respective devices, while Marsh does not explicitly show this feature, it is well known to use this type of addressing arrangement to determine which memory is to be written to read or read out of by the system (Official Notice) when plural memories are being used. Further, this arrangement is also well known when multiple memory chips are being used to constitute a single memory so as to write to the correct address. Additionally, this type of addressing scheme is also used when the memories are registers or buffers, as it, effectively, is simply a memory select which is at least conventional, if not actually inherent, in nearly all systems when memory is used to store data, as there must be a memory select to allow the memory device to be used. As to the limitations directed to the size of the data words and color (such as claim 80) the use of color is met by Marsh. The

exact size of the words is simply dependent upon routine experimentation and the desired system parameters (speed, data line sizes, the size of data that is best processed by the processor, etc.) and is not a patentable expedient as these sizes are apparently simply a matter of the components used to make up the system.

12. With respect to the dependent claims, it is firstly noted that there are apparently four different dependent claims variously dependent upon differing independent claims. These groups of claims will be treated together, below.

13. Generally, claims 22, 27, 32, 39, 47, 54, 61, 66, 71, and 76 recite substantially the same limitations. The use of a "frame buffer" in Marsh to store "a frame of display information" would have been obvious because Marsh is directed to the production of a display image and "frame buffers" are well known means to store the image data for display (Official Notice). Further, as to the recited "accessing circuit", the discussion, above, as to the use of such means also applies to these claims.

14. Generally, claims 23, 28, 33, 40, 43, 48, 55, 62, 67, 72, and 77 recite substantially the same limitations. The processing of a "kernel" of data (such as a 3x3 window of data, or other piece of data) is extremely well-known and conventional (Official Notice). To one of ordinary skill in the art, it would have been obvious, at

the time of the invention, to store the output data in a memory and to perform a kernel processing on the output data to perform a "spatial filtering" on the output image data because of the conventionality of both kernel processing and spatial filtering, particularly for processing image data prior to display of the image data.

15. Generally, claims 24, 29, 34, 41, 49, 56, 63, 68, 73, and 78 recite substantially the same limitations. The use of a "display processor" is shown by Marsh, as discussed above. The performance of a spatial filtering would have been obvious for the reasons given above.

16. As to claims 81-93, these method claims correspond to apparatus claims 21, 26, 31, 36, 45, 46, 51, 52, 58, 60, 65, 70, and 75, rejected above, and are also met by Marsh in a similar manner.

17. Claims 25, 30, 35, 42, 50, 57, 64, 69, 74, and 79, as best that they are understood, are rejected under 35 U.S.C. § 103 as being unpatentable over Marsh as applied to claims 21-24, 26-29, 31-34, 36-41, 43-49, 51-56, 58-63, 65-68, 70-73, 75-78, 80-97 above, and further in view of any of Widergren et al. (4,394,774) or Cease et al. (4,596,026) or Forquer et al. (4,491,915).

18. The interpretation of the merits of claims 25, 30, 35, 42, 50, 57, 64, 69, 74, and 79 for purposes of evaluating the claims in light of the prior art (specifically the application of Widergren et al.) was guided in part by the Board of Appeals interpretation of claims 9-14 in Parent application Serial No. 06/662,211 because claims 9-14 in the parent application are substantially similar to these present claims.

With respect to these claims, while Marsh does satisfy the claim recitation, it does not show the clocking of the writing and reading of the memories being at different clock speeds.

Widergren et al provides for a variable speed buffer (elastic buffer) wherein the rate of input data differs from the rate of the output data (note figures 2 and 17 showing the use of rate buffers 52 and 54; note also columns 10, 11 and 16). Widergren teaches a buffer for receiving information at a first word rate, storing the received information and outputting the information at a second word rate that is greater than the first rate (the rate at which information arrives at the buffer 52 is variable so that sometimes the instantaneous output word rate is greater than the variable input word rate). Further, Widergren also teaches asynchronous clocking signals (see column 17, lines 15-19) as well as having either variable rate in (changing clock pulse) and fixed rate out

(non-changing clock pulse periods) or fixed in and variable out in a variable rate controlled buffer (see Fig. 2, elements 52 and 54).

Cease et al. and Forquer et al. teach means for receiving data at a first word rate (note Fig. 2 shows asynchronous data of Cease et al; see abstract of Forquer et al); means for storing the received information (element 14 of figure 2 to Cease et al; Summary of Invention to Forquer et al); and outputting at a greater rate than the input rate (see output from element 14 in figure 2 of Cease et al - the instantaneous incoming word rate may be less than the outcoming word rate; note the abstract of Forquer et al and column 5, lines 1-57). Further, both Cease et al. and Forquer et al. provide for asynchronous input/output clocks and that the input be asynchronous and the output be synchronous (changing/non-changing pulses).

Double Patenting - 35 USC §101

19. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process . . . may obtain a patent therefor . . . " (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330

(CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

20. A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

21. Claims 95-97 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 95-97 of each of copending application Serial Nos. included in the following list:

08/464034, 08/465173, 08/465071, 08/465657, 08/463822, 08/465072, 08/469262, 08/469261, 08/469263, 08/466600, 08/466599, 08/469407, 08/471633, 08/471542, 08/469888, 08/466557, 08/470569, 08/471846, 08/469592, 08/469060, 08/471255, 08/471042, 08/471252

22. Claims 95-97 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 21, 31 and 39 of each of copending application Serial Nos. included in the following list:

08/458141, 08/456333, 08/458143, 08/458142, 08/456339, 08/457360, 08/457715, 08/457726, 08/457211, 08/457728, 08/457448, 08/457208, 08/458005, 08/458004, 08/458104, 08/456901, 08/457362, 08/456398, 08/457194, 08/457197, 08/456296, 08/456592, 08/458006, 08/457196, 08/459158, 08/460607, 08/458791, 08/459152, 08/459848, 08/460737, 08/460422, 08/460705, 08/458608, 08/460433, 08/461567, 08/459221, 08/458206, 08/460612, 08/460172, 08/458549, 08/464512, 08/464999, 08/465083, 08/461288, 08/460718, 08/460753, 08/459648, 08/464007, 08/464998, 08/469018, 08/463824.

23. These are provisional double patenting rejections since the claims have not in fact been patented.

Double Patenting - Non-statutory/Obvious-type

24. The non-statutory double patenting rejection, whether of the obvious-type or non-obvious-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel,* 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornam,* 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi,* 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman,* 29 USPQ2d 2010 (Fed. Cir. 1993).

25. A timely filed terminal disclaimer in compliance with 37 CFR 1.321 (b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78 (d).

26. Effective January 1, 1994, a registered attorney or agent of record may sign a Terminal Disclaimer. A Terminal Disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

27. Claims 21-94 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 21-94 of each of the following copending applications:

08/463823, 08/463111, 08/463821, 08/465200, 08/465199, 08/465658, 08/469321, 08/471695, 08/471553, 08/471600, 08/471701, 08/471123, 08/471425, 08/471136, 08/469580, 08/469889, 08/464034, 08/465173, 08/465071, 08/465657, 08/463822, 08/465072, 08/469262, 08/469261, 08/469263, 08/466600, 08/466599, 08/469407, 08/471633, 08/471542, 08/469888, 08/466557, 08/470569, 08/471846, 08/469592, 08/469060, 08/471255, 08/471042, 08/471252.

28. Each of these claims is identical to its equivalent claims in each of the other copending applications listed above with the exception of **1)** a single word (e.g., "window" or "moving map" or "simulator") used to describe the type of image data which is varied from application to application and **2)** the recitation of an *image memory* and/or *a database memory* in some of the applications

(i.e., claim 21 of 08/471136 recites only an image memory; claim 21 of 08/471846 recites both an image memory and a database memory; and claim 21 of 08/463822 recites neither element directly).

29. With respect to difference **1**, the Examiner takes Official Notice of the obvious and well-known nature of processing a vast variety of *types* of image data. The label applied to the image data in no way affects how it would be loaded from a memory, processed or output to a display device within the context of the claims. In other words, whether data stored in a memory is called *composite data* or *remote image data* or *filtered image data*, there is no indication that the way in which that data is handled by the claimed invention differs because of the original source of the image data. For this reason, this label applied to the term "image data" cannot patentably distinguish the claims.

30. As to difference **2**, the Examiner takes Official Notice of the obviousness of storing an image in one or more memories prior to processing. In the case of the claims which exclude any initial memory storage, the memory would clearly be an inherent and necessary part of the system as the image must exist somewhere prior to processing. As to claims which recite an additional database memory which is used to load an image memory which in turn provides image data to the processor, the exceedingly well known use of a main memory (i.e., database) and a temporary buffer memory

(i.e., image memory) show these limitations to be at most obvious variations of the embodiments which only show an image memory. Additionally, the prior patent to Marsh has previously been cited as one example of this arrangement.

31. Claims 95-97 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 8 of U.S. Patent No. 4,491,930 in view of Marsh (US 4,179,824).

32. With respect to claim 95, claim 8 of the '930 patent differs in that it recites *a signature signal* rather than *an image*, recites a *digital input means* but not the *accessing circuit* claimed in the application, and does not include the *rotation and translation processing* claimed in the application. As to the first point, it is clear that the term *signal* claimed in the patent encompass image signals (see column 263, lines 26-30 of the '930 patent). As to the second point, the inclusion or exclusion of input and memory access circuitry does not patentably distinguish the claims as such means would be recognized by one skilled in the art as necessary and inherent components of any signal processing system whether they are explicitly claimed or not (for example, the means for generating a memory output signal in the '930 patent must include some means of accessing the memory in order to function as

claimed). With respect to the translation and rotation processing, these functions are well-known types of processing (i.e., filtering) as taught by Marsh. It would have been obvious to one skilled in the art to interpret the *filter means* of the '930 patent as including such operations-- particularly in view of the statements at column 6, lines 18-25 and 36-53 of the '930 patent that broadly define the filter means as encompassing many types of digital filtering or signal processing. Note that the specification of the '930 patent is being used in this case only as a dictionary for interpreting the claim language. *In re Boylan,* 392 F.2d 1017, 157 USPQ 370 (CCPA 1968).

33. Claim 96 similarly differs from claim 8 of '930 primarily in terms of specific "image" language and the use of separate database and image memories. As discussed in the preceding paragraph, claim 8 clearly encompasses images. The recitation of a single *memory means* in the '930 patent is an obvious variation of the two separate memories claimed in the application, particularly in view of known prior art such as Marsh which makes use of multiple database and image memories (e.g., data base memory 48 in figure 1; an image memory 304, 306 in figure 3)

34. Claim 97 additionally calls for a *display means* whereas the '930 patent simply generates *an output digital signal.* Numerous

places in the '930 patent state that the output signal may be displayed on a CRT or similar display means.

Double Patenting - Non-Statutory/Non-Obvious-type

35. Claims 21-97 are rejected under the judicially created doctrine of double patenting over claims 21-97 of each of the copending applications listed below:

08/464034, 08/465173, 08/465071, 08/465657, 08/463823, 08/463822, 08/465072, 08/463111, 08/463821, 08/465200, 08/465199, 08/465658, 08/469262, 08/469261, 08/469263, 08/466600, 08/466599, 08/469407, 08/471633, 08/471542, 08/469321, 08/471695, 08/471553, 08/471600, 08/471701, 08/471123, 08/471425, 08/471136, 08/469580, 08/469889, 08/469888, 08/466557, 08/470569, 08/471846, 08/469592, 08/469060, 08/471255, 08/471042, 08/471252

36. The subject matter claimed in the instant application is fully disclosed in the referenced copending applications and would be covered by any patent(s) granted on those applications since the instant application and each of the referenced copending applications claim common subject matter. Full support for any of claims 21-97 can be found in any of the referenced applications since each specification is identical. Furthermore, claiming of common subject matter is evidenced by the considerable overlap of claims among various ones of the referenced applications. For example, claim 88 of 08/471600 is identical to claim 89 of 08/471701, claim 90 of 08/471123 and claim 91 of 08/471425. Numerous other similar examples can be found.

37. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending applications. *In re Schneller,* 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP §804.

38. Claims 21-94 are rejected under the judicially created doctrine of double patenting over claims 25, 26-28 and 58 of U.S. Patent No. 4,954,951 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

39. The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

40. Representative claim 21 in the instant application recites "an image processing system **comprising**" (emphasis added) an image memory, a processor, a plurality of memories including first, second and third memories, an input circuit and first and second output circuits. These elements are covered by claim 25 of the patent which calls for a "memory system **comprising**" (emphasis added) an image memory and a plurality of memories including a first, second and third memory ("a plurality of integrated circuit memory chips . . . storing data," lines 2-3) an input circuit

("address generator circuit," line 4), and output circuits ("a scanout circuit," lines 9-12). The specific use of "image information" is disclosed in the specification at, for example, column 8, lines 49-59. The use of multiple output/buffer circuits is discussed at, for example, columns 239-240.

41. The use of the various descriptive labels identifying particular *types* of image data are variously supported in the disclosure of the '951 patent or in the disclosures of the applications incorporated by reference. For example, column 10, lines 47+ discuss windows; column 10, lines 66+ discuss anti-aliasing and filtering; and virtually any of the images discussed could be termed "informational."

42. The other independent claims in the instant application recite similar combinations of elements containing common subject matter to that claimed in the patent and supported by that specification. For example, claim 28 of the patent recites *a processor coupled to the memory* . Claim 27 of the patent calls for an *accessing circuit* as recited in claims 58 and 60 (for example) in the instant application. Claim 58 of the patent calls for a *selection circuit* as recited in (for example) claim 37 of the instant application.

43. Representative dependent claims 22-25 also claim subject matter common to claims in the patent and fully supported by the patent specification. For example, the *accessing circuit* recited

in application claim 22 corresponds claim 27 of the patent. The *kernel memory* and *kernel processor* of claim 23 is broadly covered by the *processor* in claim 28 of the patent and further supported by the discussion of window generation and processing in column 10 of the specification. The *spatial filtered* data in claim 24 is supported by lines 65+ of column 10 in the specification and broadly covered by the *processor* of claim 23. The first and second clock circuits of claim 25 correspond to the *addressing* at *first and second address update* rates claimed in claim 26. The remainder of the dependent claims contain analogous limitations which similarly correspond to subject matter covered by the '951 patent.

44. The additional limitations of "an image memory" and/or "a database memory" recited in some of the claims are broadly encompassed by the recitation of "a memory storing data" in the '951 patent.

45. Since the transitional phrase "comprising" does not exclude the presence of elements besides those explicitly claimed, the patented claims already cover the additional limitations disclosed in the patent specification but not claimed. Hence, the patent protection for the subject matter claimed in the patent would be extended by the allowance of the claims in the instant application.

46. Furthermore, there is no apparent reason why Applicant was prevented from presenting claims corresponding to those of the

instant application during prosecution of the application which matured into patent 4,954,951. *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP §804.

Conclusion to Double Patenting Rejections

47. While it is true that the Examiner has the burden to show how a rejection is specifically applied to each claim, the exemplary showing with respect to the claims individually discussed above is enough to give the applicant fair notice of how the rejection is applied to each and every other claim. The above paragraphs establish a prima facie showing of the unpatentability of the instant claims and the burden shifts to the applicant to show, if he can, patentable distinctions between the instant claims and those of the other applications and patents.

48. The drawings are objected to under 37 C.F.R. § 1.83(a). The drawings must show every feature of the invention specified in the claims. Applicant's claims recite a number of embodiments of the invention. However, no embodiment appears to be shown in its entirety in any of the drawings, and therefore the structural relationships between elements as recited in the claims are not shown in the drawings. In addition, the claims recite a number of embodiments which process or generate particular types of images.

The drawings do not show the specific embodiments of the invention which process or generate the following types of images: rotated, translated, scaled, perspective, antialised, scanned out, filtered, occulted, range-related and database. If Applicant believes every claimed feature as indicated above is present in the drawings, in his response to this objection, he should point out the specific figures and elements in the drawings which show these features. These features must must be shown or the features cancelled from the claims. No new matter should be entered.

49. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Swanson et al. (4,496,976) and Goldberg (4,412,230) disclose various systems that show the conventional use of buffers and double buffers. Preiss et al.(4,672,369) discloses a display system that uses various memories.

Contact Information

The following Examiners were involved in the preparation of this Office Action:

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If attempts to reach the Examiner(s) by telephone are unsuccessful, the team supervisor, Michael Razavi, can be reached at (703) 305-4713.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-8576.

The Art Unit FAX number is (703) 308-6606.

LJP JC BS

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ART UNIT 266